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APPLICATION NOTE

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REFLECTING ON TRANSMISSION LINE EFFECTS

This application note describes introductory transmission line characterization, analysis, and application. Over the past couple of years, microprocessors and digital logic in general have seen substantial increases in line drive capability. This increase has fostered the current logic and microprocessor speeds readily available today. The relatively quick rise and fall time of today's digital devices makes an understanding of transmission lines and their effects on system reliability a necessity.

TRANSMISSION LINE CHARACTERIZATION

When discussing transmission lines one should reflect on the following definition. A transmission line is two or more conductors separated by some insulating medium, used to carry a signal. At first glance this seems rather trivial, but upon closer examination one finds a host of physical nuances which make the transmission line a sophisticated element to describe, among which are:

1. Line resistance present in any non-ideal conductor.
2. Line conductance ((1/R) = G) present in any non-ideal insulating medium resulting in leakage currents.
3. Line inductance present in any current carrying conductor undergoing a change in magnetic flux.
4. The line capacitance present between the two conductors separated by the insulating medium.

Figure 1 shows the line under discussion. The circuit consists of two series elements (Z + L) and two shunt elements (C + G).

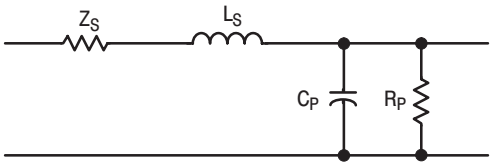

Figure 1. Transmission Line Circuit

Our discussion will be primarily concerned with C + L, because these elements are the frequency dependent components of the line (neglecting skin effect). For frequencies above approximately 100 kHz, Z_o, the characteristic impedance of the line, is equal to the square root of L/C and is independent of line length. The propagation constant (t_{pd}) or time delay constant is the square root of L*C, and is a function of line length. Z_o is of particular importance to our discussion because when you match this impedance to the load, you reduce the effects of transmission imparted to both the source and the load.

TRANSMISSION LINE REFLECTIONS

Reflections on a line are caused by a mismatch in impedance between the line and the load. If all the power delivered to the line is absorbed by the load then there will be no reflected power back at the source side of the line. This principle of power conservation is the cornerstone of this application note. Refer to Figure 2 as the equations are discussed. The equation describes the ratio of absorbed power to reflected power based on the ratio of line to load impedance.

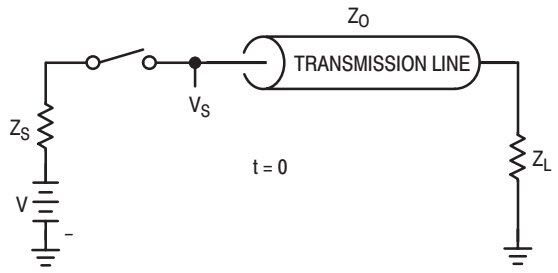

Figure 2. Transmission Line

The current delivered to the load is $I_L = I_{INC} - I_{RFL}$ (incident current minus reflected current), while the load voltage is, $V_L = V_{INC} + V_{RFL}$ (incident voltage plus reflected voltage). We need to find an equation that relates incident voltage to reflected voltage. Therefore noting that the load current $I_L = (V_F - V_{RFL})/Z_o$ (incident voltage minus reflected voltage divided by the characteristic impedance) we can see the following relationship.

$$\frac{V_{INC} + V_{RFL}}{Z_L} = \frac{V_{INC} - V_{RFL}}{Z_o} \quad (1)$$

Solving for V_{INC}/V_{RFL}

$$Z_o (V_{INC} + V_{RFL}) = Z_L (V_{INC} - V_{RFL}) \quad (2)$$

$$V_{RFL} (Z_o + Z_L) = V_{INC} (Z_L - Z_o) \quad (3)$$

$$\frac{V_{RFL}}{V_{INC}} = \frac{Z_L - Z_o}{Z_L + Z_o} = \rho_L \quad (4)$$

This expression is called the load reflection coefficient (ρ_L). Note a ρ_S also exists which relates the ratio of source impedance to line impedance. This expression is called the source reflection coefficient and is shown in Equation 5.

$$\rho_S = \frac{Z_S - Z_o}{Z_S + Z_o} \quad (5)$$

One can see that there are three distinct possibilities which require inspection. First, the situation where the load impedance equals the line impedance ($Z_L = Z_o$) and $\rho_L = 0$ (no reflections — a properly terminated line); second, where the load impedance is greater than the line impedance ($Z_L > Z_o$) and ρ_L is positive, generating a reflection whose polarity matches that of the incident voltage, and, finally, where the load impedance is less than the line impedance and ρ_L is negative, generating a reflection whose polarity is opposite

to that of the incident voltage. Let's take a closer look at the last two cases.

Assume that $Z_L = 4Z_o$, and that the source impedance = line impedance. V = source voltage, and V_L = load voltage (see Figure 3).

$$\rho_L = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{4Z_0 - Z_o}{4Z_o + Z_o} = 0.6$$

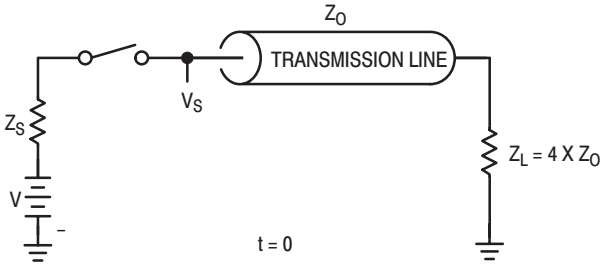

Figure 3. Transmission Line Circuit with $Z_L = 4 * Z_o$ and $Z_s = Z_o$

Thus at t = 0 a voltage wave of 1/2(V) (because Z_S and Z_o form a voltage divider on V) begins to travel down the line and arrives at Z_L one t_{pd} or propagation delay later. When the wave encounters the load impedance mismatch, a reflected wave equal in magnitude to (V/2)*0.6 is reflected back toward the source, and arrives at the source again one t_{pd} later. This causes the voltage at the source to rise therefore creating the classic overshoot condition.

Since the source and line impedance are matched no further reflections are generated and the line has reached its steady state condition. See Figure 4.

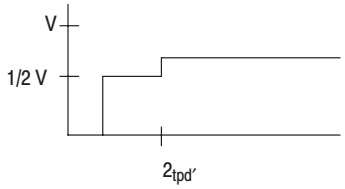

Figure 4. Voltage versus Time Plot of $Z_L = 4 * Z_o$ and $Z_s = Z_o$

The next scenario is when $Z_L < Z_o$. For this case assume the following conditions. $Z_L = Z_o/4$ and $Z_S = Z_o$. See Figure 5.

$$\rho_L = \frac{.25Z_0 - Z_o}{.25Z_o + Z_o} = -0.6$$

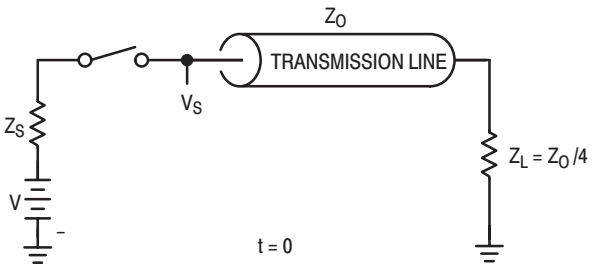

Figure 5. Transmission Line Circuit with $Z_L = Z_o/4$ and $Z_s = Z_o$

At time t = 0 a voltage wave equal in magnitude to 1/2V begins to travel down the line arriving at the load one delay time later. The impedance mismatch generates a reflected wave equal in magnitude to the reflected wave discussed in the first example, but opposite in polarity. At time $2t_{pd}$ this wave reaches the source and sums with the existing voltage present from time t = 0 (V/2), reducing its value to $V_s/5$ or ((V/2)(– 0.6) + V/2). This is the classic undershoot condition. See Figure 6.

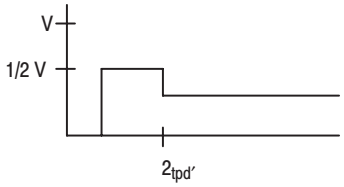

Figure 6. Voltage versus Time Plot of $Z_L = Z_o/4$ and $Z_s = Z_o$

At this point we need to reflect on one of the equations described earlier. The equation states that $V_L = V_{INC} + V_{RFL}$. We can see this holds true as noted in the preceding examples, where V_L and V_S either increased or decreased with corresponding mismatches in impedance.

THE LATTICE DIAGRAM

The lattice diagram permits a network to be checked quickly for balance (match). The diagram is essentially a two-line graph with corresponding source and load impedance, connected by a reflection diagonal with a period of $2t_{pd}$ (twice the line delay time). This diagonal is used to represent the reflected voltage's magnitude. See Figure 7.

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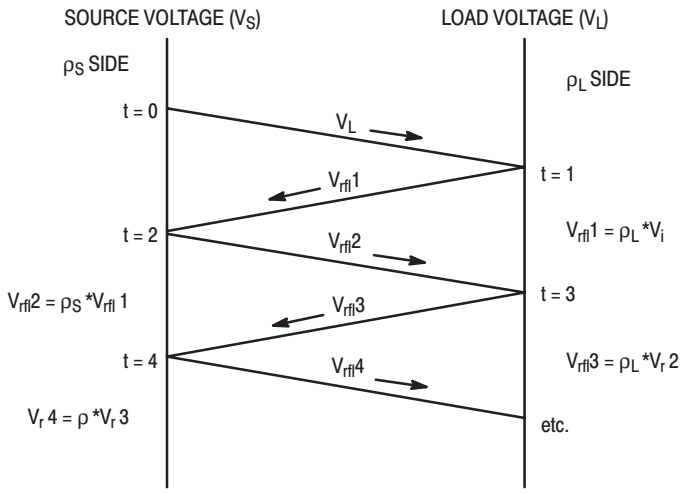

Figure 7. Lattice Diagram

The example below will illustrate the use of the lattice diagram. For the analysis assume the following circuit (see Figure 8 and 9).

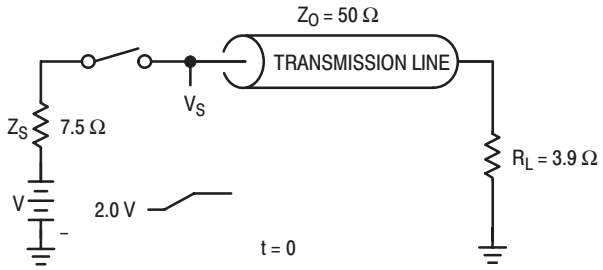

Figure 8. Transmission Line Circuit for $Z_s = 7.5\ \Omega$, $Z_o = 50\ \Omega$ and $Z_L = 3.9\ \Omega$

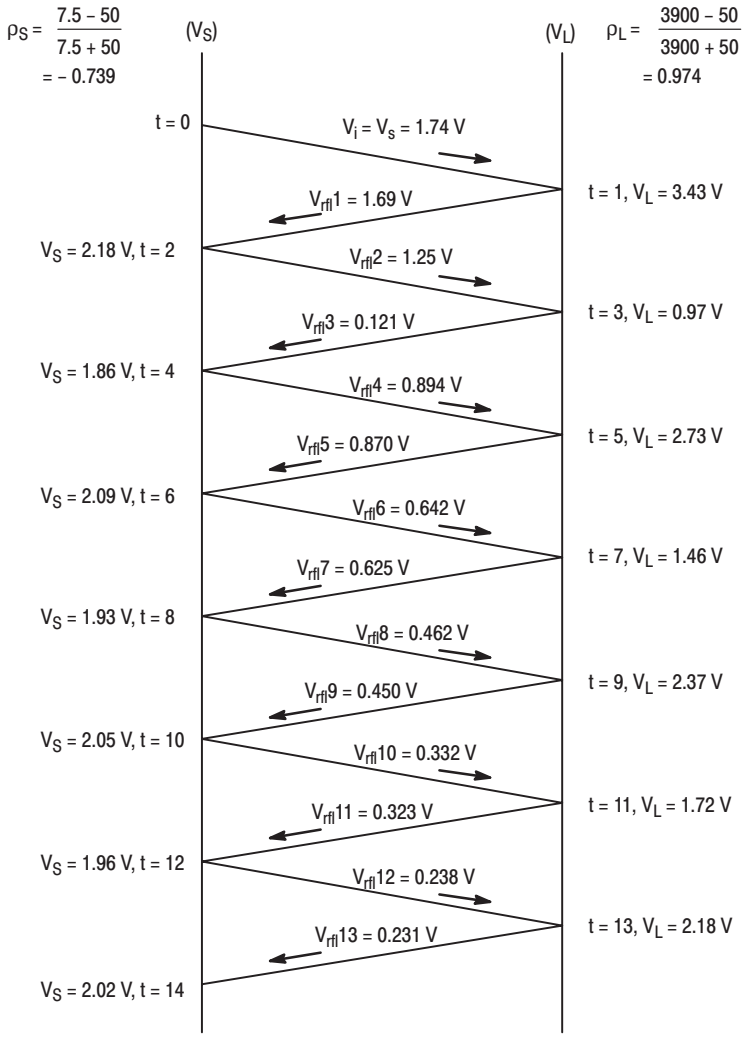

Figure 9. Lattice Diagram for Z_S = 7.5 Ω, Z_o = 50 Ω and Z_L = 3.9 Ω

Transmission Line Types

There are essentially two types of transmission lines; the microstrip and the stripline. The microstrip is shown in Figure 10. It consists of a conductor separated from the ground plane on one side by a dielectric.

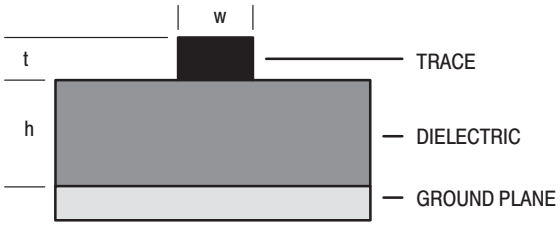

Figure 10. MIcrostrIp Transmission Line

The characteristic impedance of a one ounce line configured as a microstrip on G-10 fiber glass is:

$$Z_o = \frac{87}{\sqrt{E_R + 1.41}} * \frac{\text{Ln}\,(5.98h)}{(0.8w + t)} \qquad (6)$$

t = 0.0015 in. for 1 oz. copper

= 0.0030 in. for 2 oz copper

h = 0.062 in. for G-10 glass epoxy

w = design dependent (based on current handling requirements.) = 0.015 in.

For our discussion,

E_R = 4.7 – 5.3

For this example, with E_R = 4.7, Z_o = 116.6 Ω

The unloaded propagation delay

$t_{pd} = 1.017 \sqrt{0.475E_R + 0.67}$ ns/ft = 173 ns/ft.

The stripline is a conductor separated from ground on two sides by a dielectric (see Figure 11).

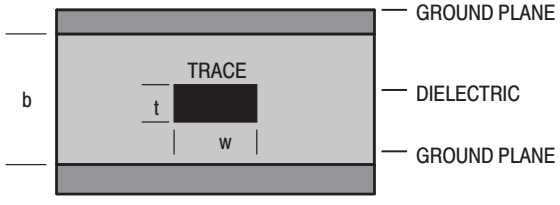

Figure 11. Stripline Transmission Line

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The characteristic impedance of G-10 fiber glass board trace configured as a stripline is:

$$Z_o = \frac{60}{\sqrt{E_R}} * \mathrm{Ln}\left[\frac{4b}{067\pi\,(0.8w + h)}\right] \quad (7)$$

Using the same parameters as above we find that Z_o = 60 Ω. The propagation delay =1.017 $\sqrt{E_R}$ = 2.20 ns/ft.

Loaded Transmission Line Propagation Delay and Impedance

As stated earlier the unloaded propagation of a microstrip line is:

$$t_{pd} = 1.017\ \sqrt{0.475E_R + 0.67}\ \text{ns/ft}$$

This delay increases with capacitive loading. The increase is equal to $\sqrt{1 + C_D/C_o}$ where C_D is the distributed capacitance and C_o is the intrinsic capacitance of the line. C_o is obtained from Figure 3-8 of Reference 1, or alternatively it can be calculated as $C_o = t_{pd}/Z_o$. For the microstrip described above with thickness (h) of 0.062 in, and signal trace width of 0.015 in, C_o = 15 pf. Assuming this line is loaded with five 10 pf loads the loaded propagation delay becomes:

$$(1.73\text{ns})\ \sqrt{1 + 50/15} = 3/60\ \text{ns/ft}$$

The loaded line impedance $Z_o' = Z_o/\sqrt{1+ C_D/C_o}$ = 116.6/2.08 = 56 Ω.

For the stripline discussed above there is a corresponding increase in t_{pd} and Z_o.

The loaded propagation delay $t_{pd}' = 2.2\ \sqrt{1 + 50/15}$ = 4.57 ns/ft, while the loaded impedance $Z_o' = 60/\sqrt{1 + 50/15}$ = 28.8 Ω.

It is apparent that capacitive loading increases the propagation delay of the line while decreasing its impedance.

TRANSMISSION LINE TERMINATION

No discussion about transmission lines would be complete without examining the techniques to properly terminate a line. Essentially there are three (3) methods which can be employed. They are:

1) Unterminated line (controlling board parameters to match line and load impedance).
2) Series termination.
3) Parallel termination.

Unterminated Line Method

This method involves controlling the length of the line such that any reflections caused by the load are absorbed by the rise and fall time, t_r and t_f of the driving gate. For this method to be effective the propagation delay (loaded delay) of the line must be short relative to t_r and t_f. This allows the reflected wave to sum with the rising or falling driving gate waveform. If four times the propagation delay of the line is less than or equal to t_r or t_f, then minimal ringing (overshoot, undershoot) will be observed. Specifications for t_r and t_f for various logic families are readily available. Knowing these times one can set the maximum line length such that the lines $t_{pd}' <= t_r/4$. For distributed loads that are stubbed, the length of the stub should be set to minimize any reflections. A t_r/t_{pd}' ratio greater than 8:1 should suffice.

Series Termination

In series termination a resistance is inserted between the driving gate output and the line. The combined output impedance of the driving gate plus the added series resistance is selected to equal the loaded impedance of the line. Since the input impedance of the driven gate is much greater than Z_o, the line will ring. Basically this termination configuration will ring once and reach steady state within $2t_{pd}'$. End of line loading, (lumped loading) is the only method of loading that is recommended for this type of termination. This is because any distributed load on the line "sees" a voltage equal to v/2 until steady state. This condition could violate the valid V_{IH} or V_{IL} specification of these gates. Clearly distributed loads are to be avoided. Receivers at the end of the line will not experience this condition, as the incident voltage and the reflected voltage add together to equal the load voltage (V_L) one t_{pd}' after the signal is asserted.

Parallel Termination

In the parallel termination method two resistors are placed at the end of the line. One resistor from the line to ground, and the other from the line to V_{CC}. The parallel combination of these resistors is set to be equal to the loaded impedance of the line. For example, if Z_o' of the line is equal to 50 Ω, then the parallel combination of both resistors should equal 50 Ω. Note this method of termination requires more drive current. The driver selected must be able to handle the additional load placed upon it by the added parallel load. Also it is apparent that this method of termination consumes power even in the steady state, as an additional current path has been set up between V_{CC} and ground.

A PRACTICAL EXAMPLE

Upon completing the paper design for our new project, we begin to peruse our schematics for possible transmission line problems. For the purposes of our discussion assume the following configuration:

V_{CC}	5 volts
PC trace	microstrip configuration, G-10 fiber glass, 1 oz. copper, E_R = 4.7, w = 0.015, t = 0.0015, h = 0.062
Logic family:	Fast TTL (drive and receive side of line)
Driving gate:	F241 buffer
$t_f + t_r$ F241:	2 ns (for 50 pf lumped load)
Number of loads (F08's):	5 (input capacitance = 5 pf/load) (I_{IL} = 600 μa, I_{IH} = 100 μa)
Configuration:	Distributed loads approximately every 2 in. for a total trace length of 10 in.

Procedure

1. Calculate the lines characteristic impedance (Z_o).
   Z_o = same as example described earlier = 116 Ω.
2. Calculate unloaded propagation delay (t_{pd}).
   $t_{pd} = 1.017\ \sqrt{0.475E_R + 0.67}$ =1.73 ns/ft
3. Calculate the lines intrinsic capacitance (C_o)
   $C_o = t_{pd}/Z_o$ expressed as nf/ft
   C_o = (1.73 ns/ft)/116 = 15 pf/ft = 1.25 pf/in. * 10 in. = 12.5 pf

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4. Calculate the loaded line impedance (Z_o')

   $Z_o' = 116 \sqrt{1.25/12.5} = 67\ \Omega$

5. Calculate the lines loaded propagation delay (t_{pd}')

   $t_{pd}' = 1.73 \sqrt{1 + 25/12.5}$

   t_{pd}'= 3.0 ns/ft = 0.25 ns/in. * 10 in. = 2.5 ns which is greater than $t_r/4$

As described earlier, since the loaded propagation delay of the line exceeds $t_r/4$, we will have to terminate the line. The loads are not lumped at the end of the line, they are distributed. As explained earlier, series termination cannot be used because of the possible threshold violations. For this example we will use parallel termination. The parallel resistor combination will be chosen to match the loaded impedance of the line. Noting the drive current of the F241, (I_{OL}= 64 ma, I_{OH}= 15 ma), we can set the source current resistor equal to:

$$V_{OH}\ (min)/((5*100\ \mu a) + I_{OH}/2) = 2\ V/8\ ma = 250\ \Omega$$

Note: $I_{OH}/2$ arbitrarily chosen. Value could be reduced if required.

The sink current resistor part of this terminator is equal to 91 Ω. This results in a drive sink current equal to:

$$(Number\ of\ Loads * I_{IH}) + V - V_{OL}\ (F241)/91 = 5 * 600\ \mu a + 5v - .55V/91\ \Omega = 52\ ma$$

Note: Weight the source side terminator such that both sink and source current specification are not violated. As shown the parallel combination of the terminating resistors is set equal to the loaded line impedance. See Figure 12.

Since the line is now properly terminated, reflections will be minimized.

In this example, the loads were not stubbed. Had they been located on a stub, an extra calculation would have had to been performed to ascertain the maximum permissible stub length.

This calculation runs as follows:

1. Set $t_r/t_{pd}' = 8.5$ and solve for t_{pd}'

   $t_{pd}' = 2\ ns/8.5 = 235\ ps$

2. Solve for the maximum stub length (x)

   $235\ ps = 1.73\ ns/ft \sqrt{1 + 5\ pf/(x)in./1.25\ pf/in.}$

   $235\ ps = 144\ ps/in. \sqrt{1 + 4/x}$

   $X\ t_{pd} = 1.017 \sqrt{0.475E_R + 0.67} = 1.73\ ns/ft = 2.42\ in.$

REFERENCES

1. *MECL System Design Handbook*, Motorola Inc., 4th ed., 1988.
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3. *The Interface Handbook Line Drivers and Receivers Interface*, Fairchild Semiconductor, 1st ed., 1975.

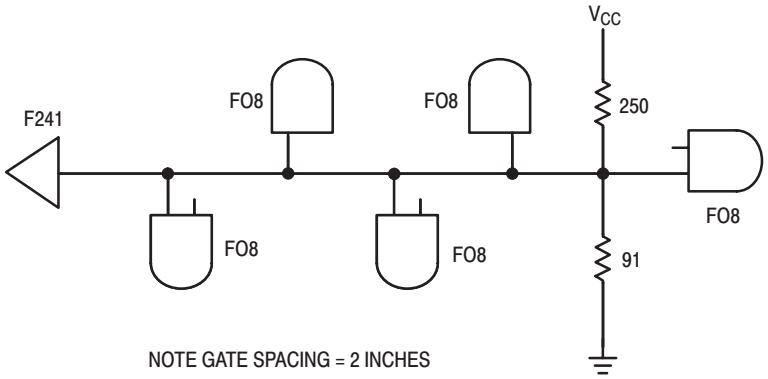

Figure 12. Transmission Line — Example

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